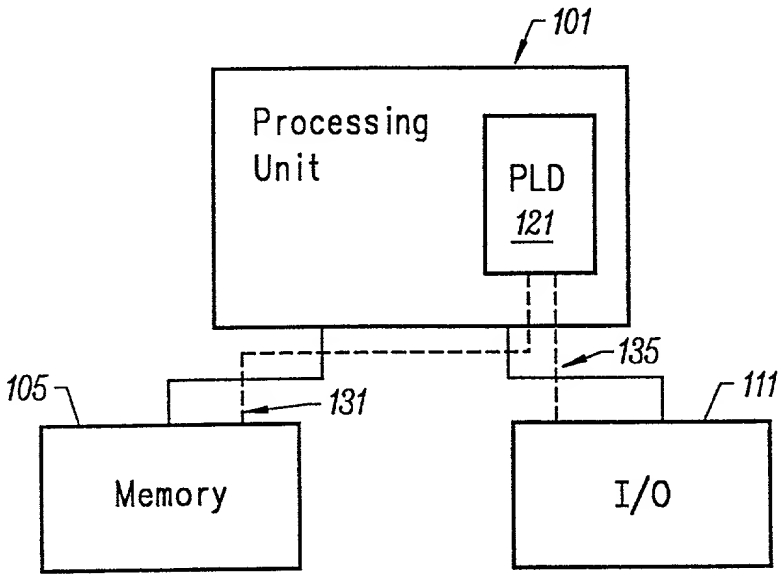


FIGURE 1

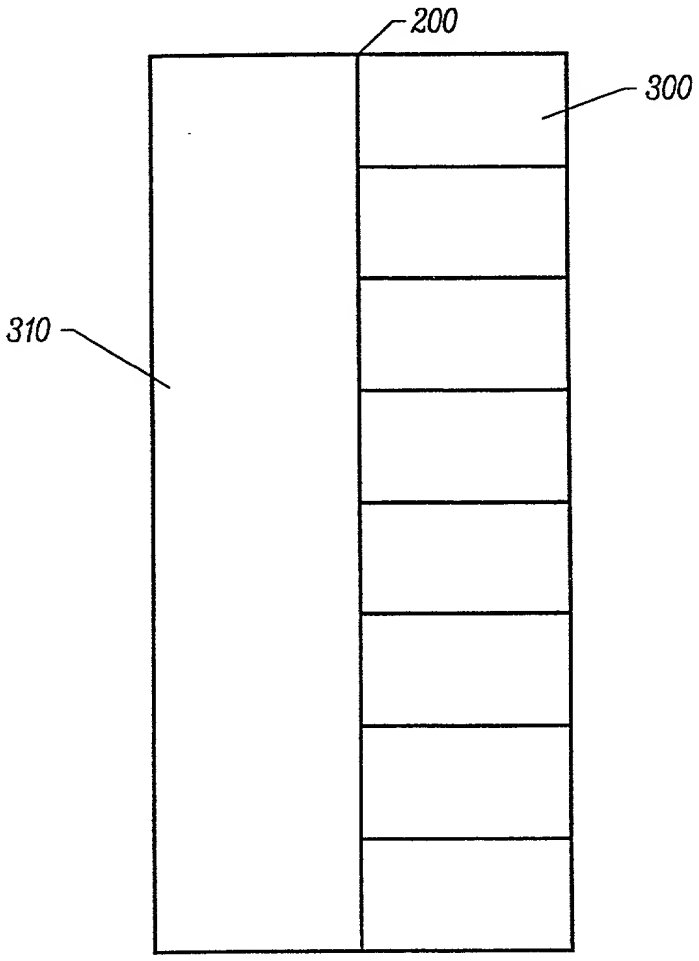
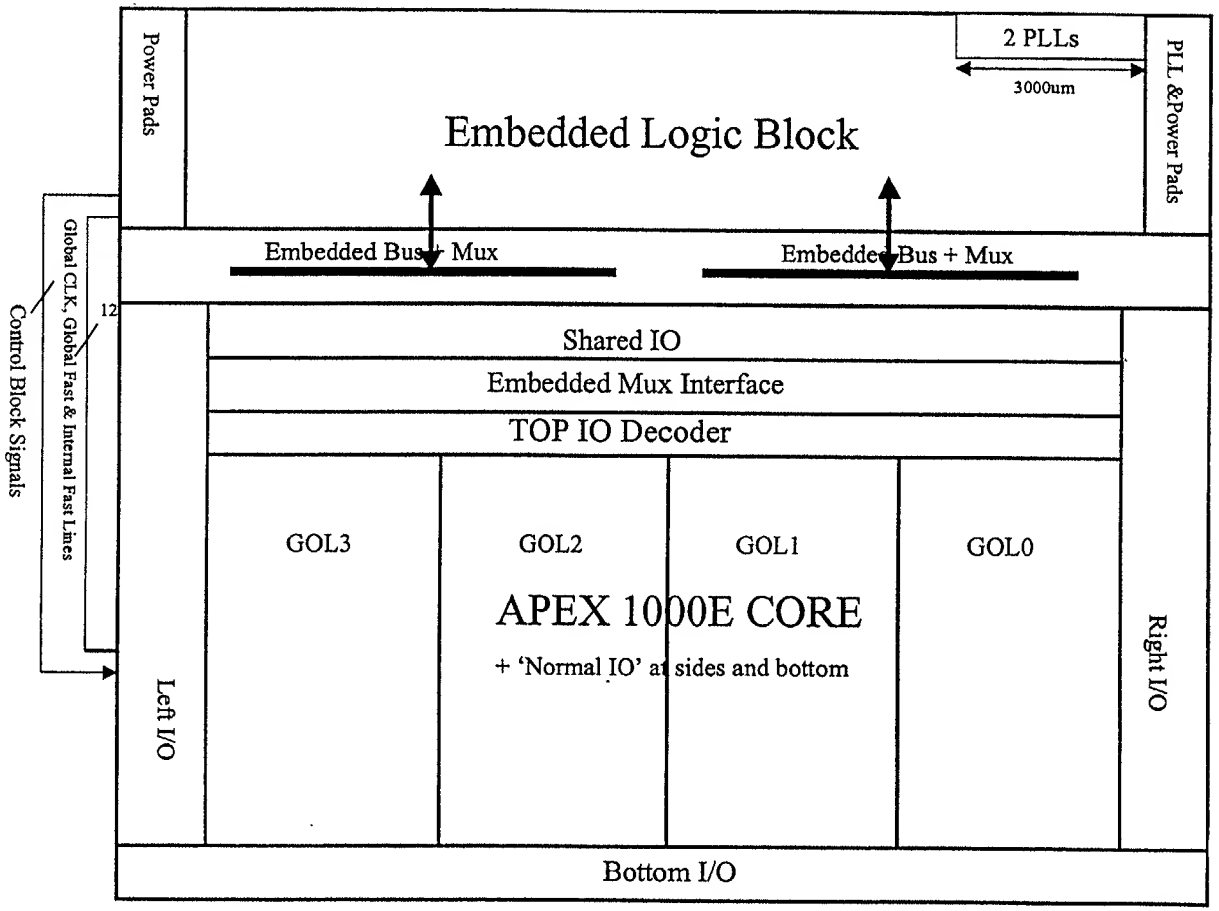


FIGURE 4



Top Level Floorplan

FIGURE 2

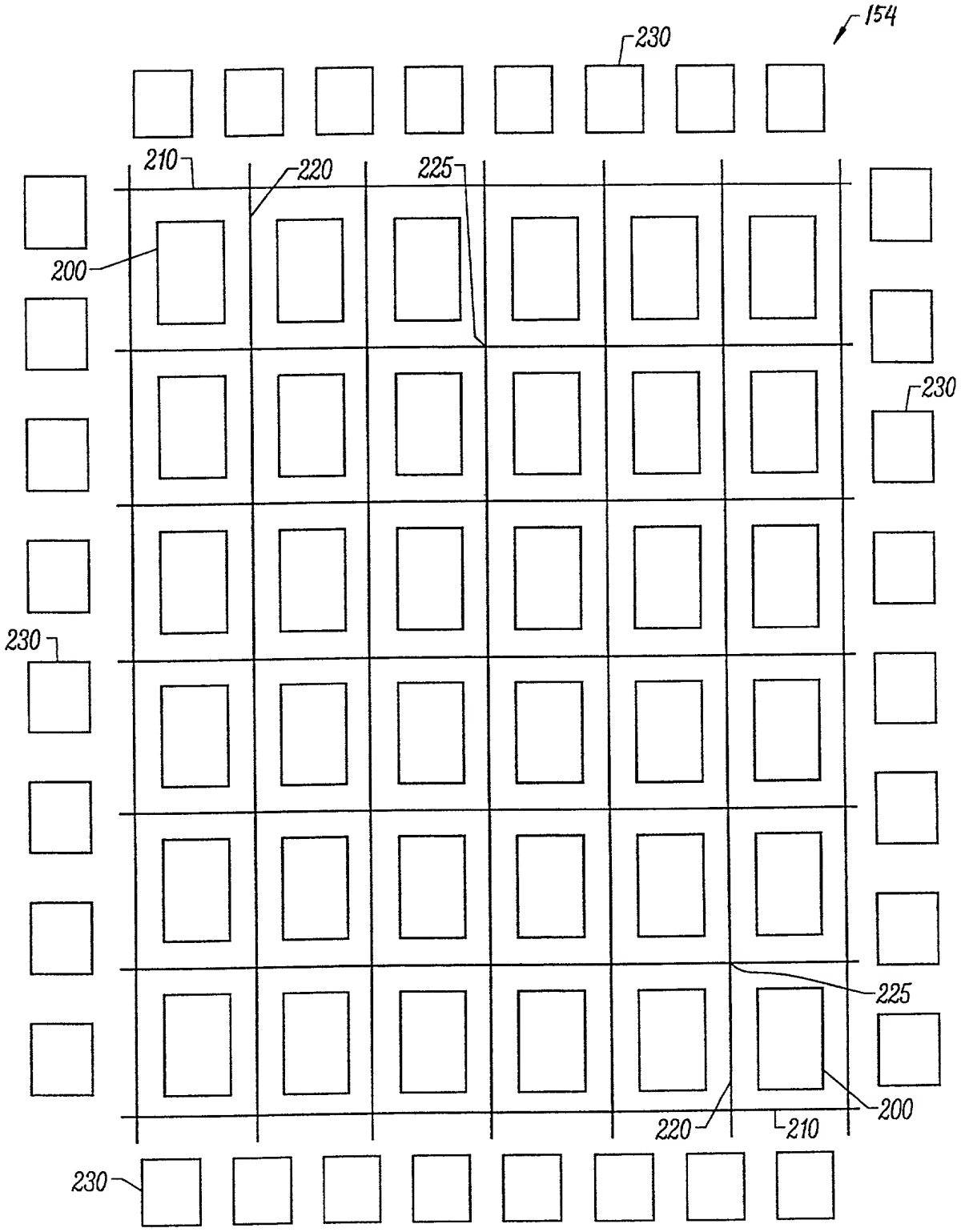


FIGURE 3

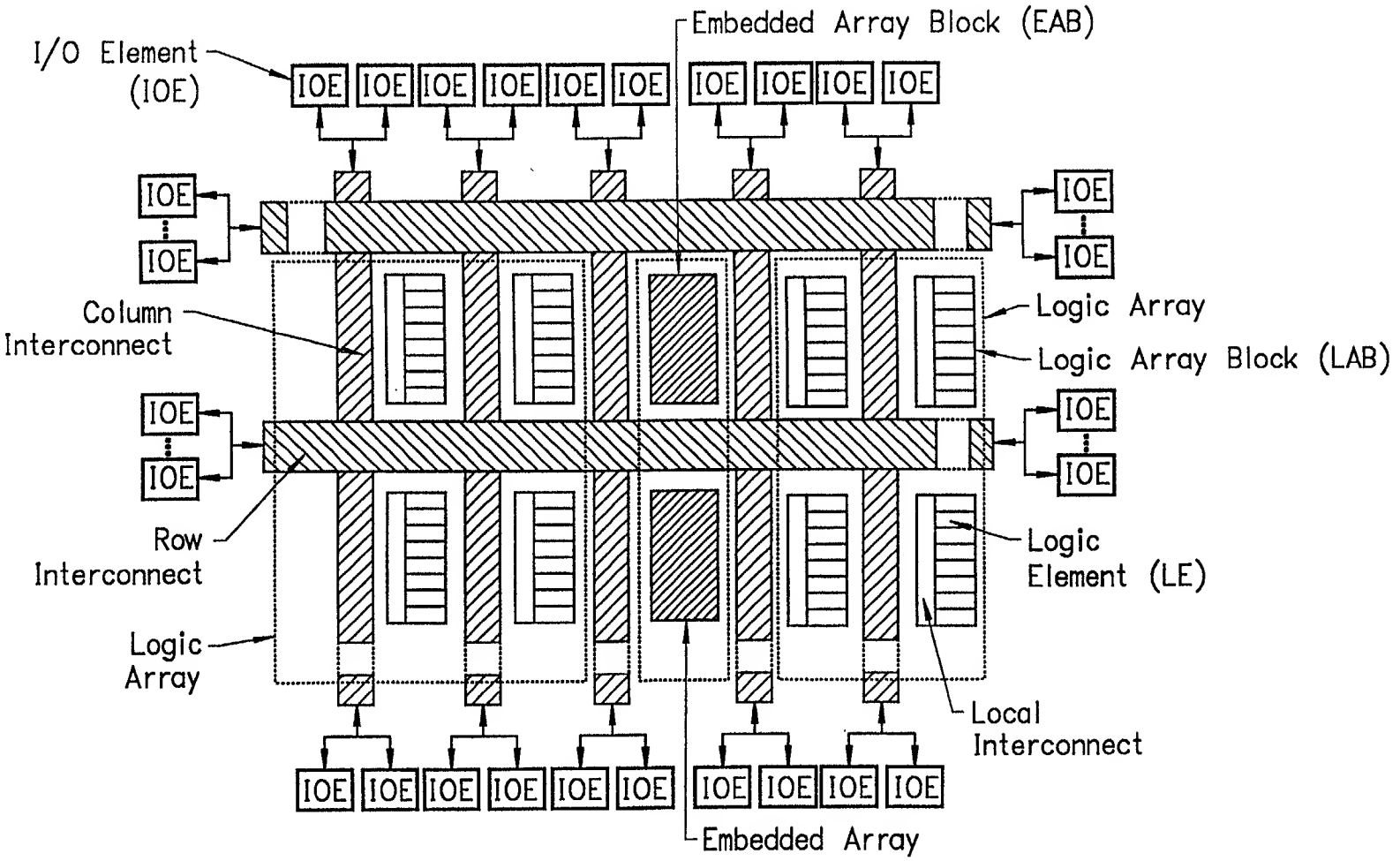

I/O Element
(IOE)
Embedded Array Block (EAB)
IOE
Column
Interconnect
Logic Array
Logic Array Block (LAB)
Row
Interconnect
Logic
Element (LE)
Logic
Array
Local
Interconnect
Embedded Array

FIGURE 5

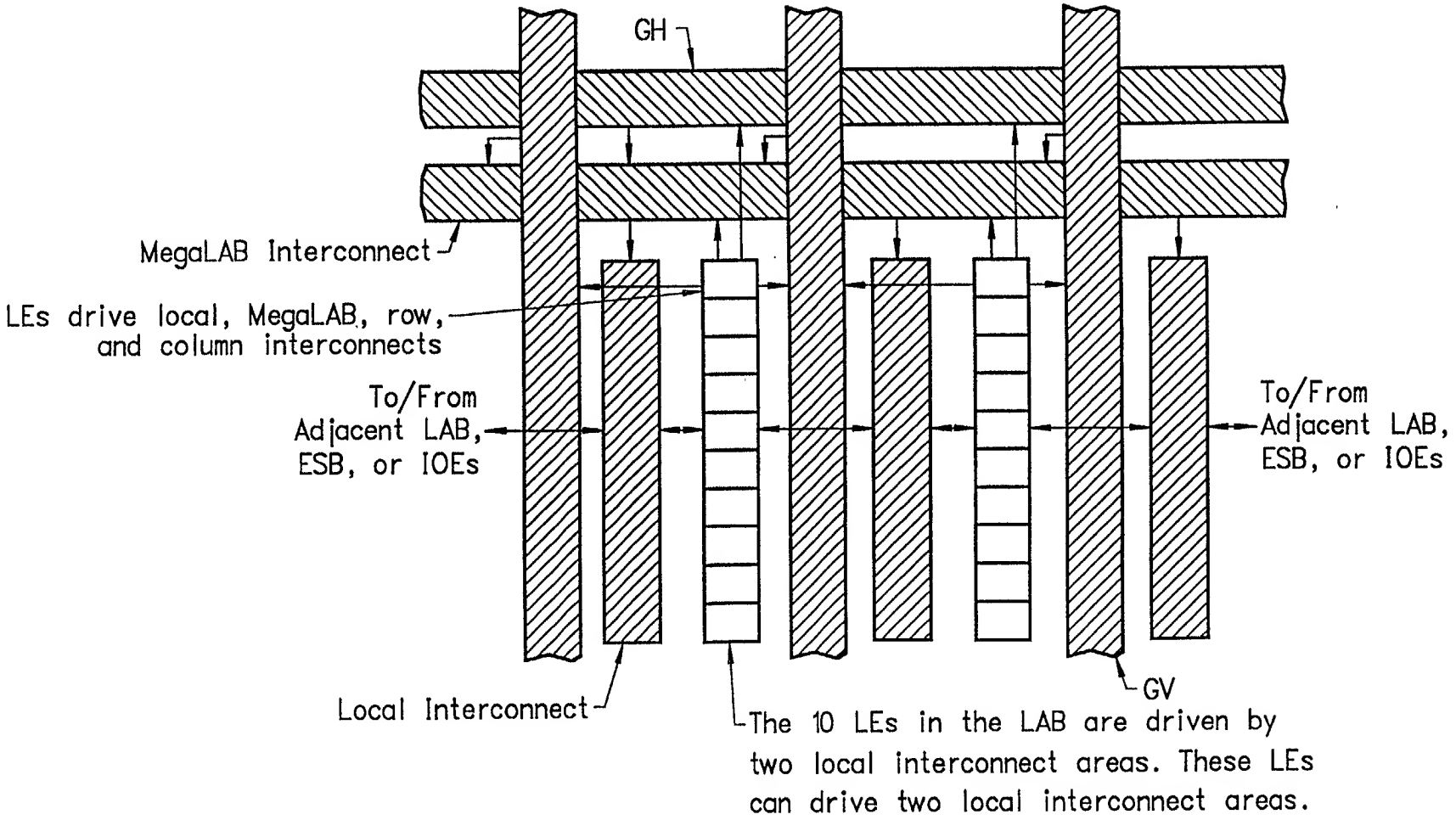


FIGURE 6

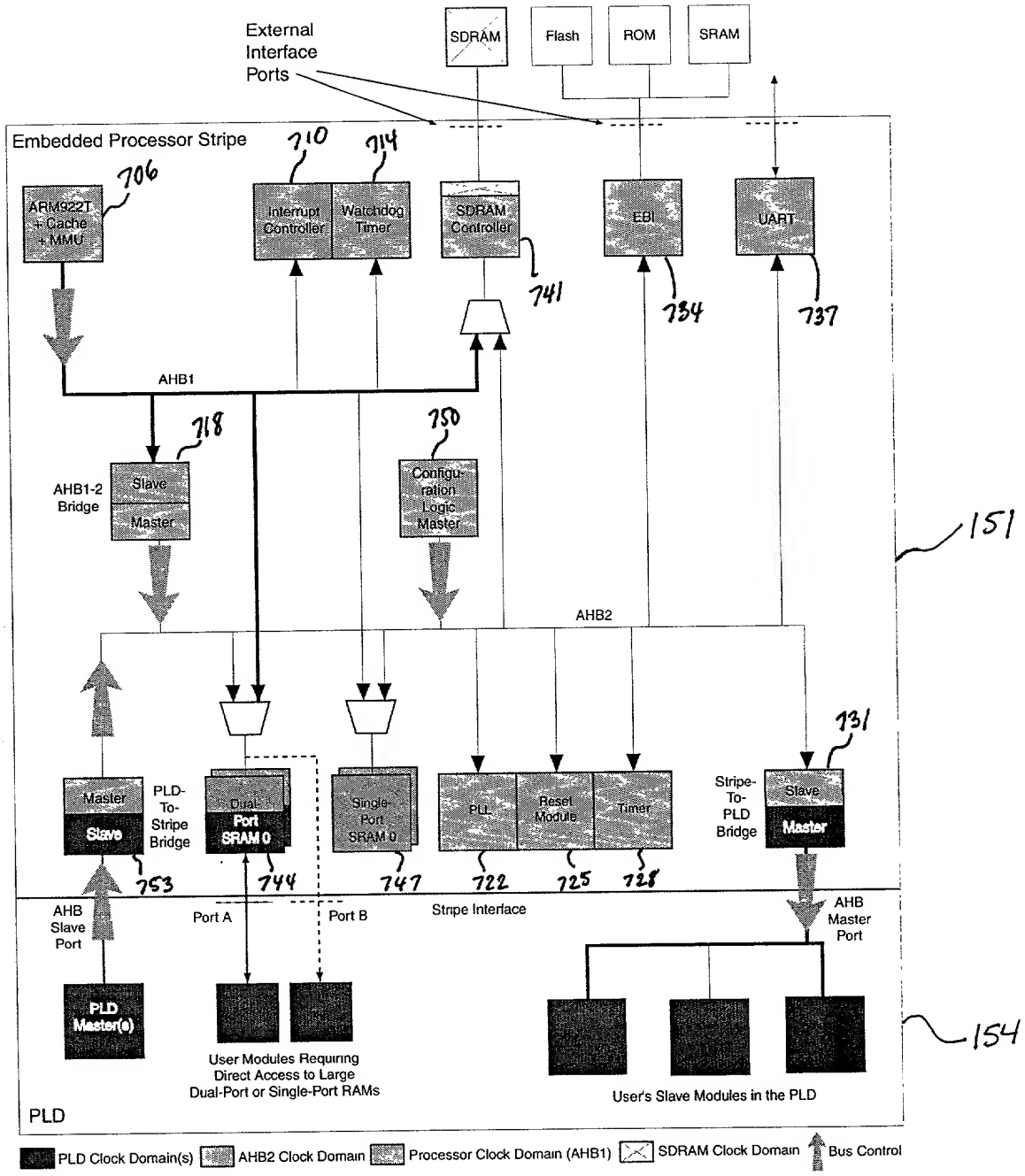

External Interface Ports
SDRAM
Flash
ROM
SRAM
Embedded Processor Stripe
710
714
706
ARM922T + Cache + MMU
Interrupt Controller
Watchdog Timer
SDRAM Controller
741
EBI
734
UART
737
AHB1
718
750
AHB1-2 Bridge
Slave
Master
Configuration Logic Master
151
AHB2
131
Master
Slave
PLD-To-Stripe Bridge
753
Dual-Port SRAM 0
744
Single-Port SRAM 0
747
PLL
Reset Module
Timer
722
725
728
Stripe-To-PLD Bridge
Slave
Master
AHB Slave Port
Port A
Port B
Stripe Interface
AHB Master Port
PLD Master(s)
154
User Modules Requiring Direct Access to Large Dual-Port or Single-Port RAMs
User's Slave Modules in the PLD
PLD
PLD Clock Domain(s)
AHB2 Clock Domain
Processor Clock Domain (AHB1)
SDRAM Clock Domain
Bus Control

FIGURE 7

FIGURE 8

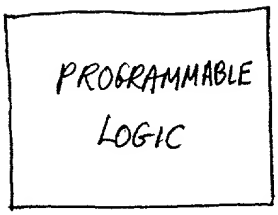


FIGURE 9

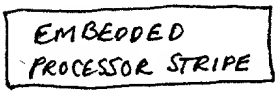


FIGURE 10

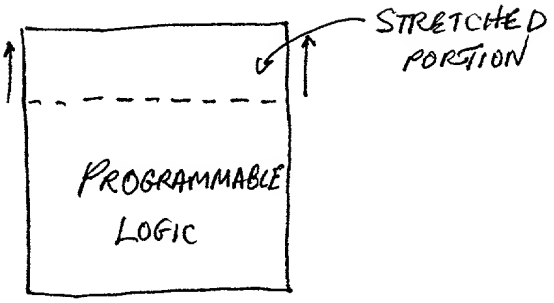
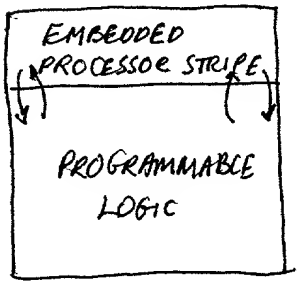


FIGURE 11



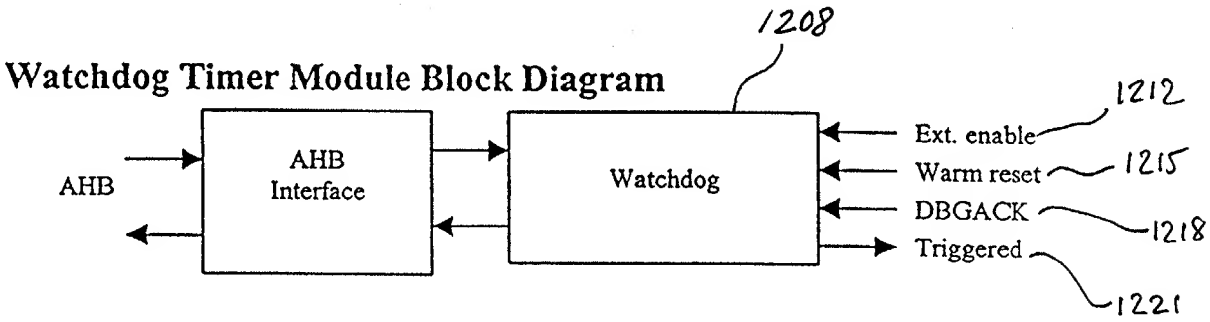


FIGURE 12

Control Register (WDOG_CR) – Read/Write

Register : WDOG_CR Address : Address Base + 0x4C0 Access: Read/Write

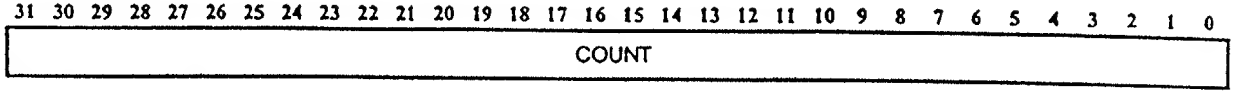
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																TRIGGER												0			LK

LK	R/W	When this bit has the value 1 further writes to the register have no effect.
TRIGGER	R/W	0 means watchdog disabled. Other values specify bits 29:4 of the trigger value (bits 3:0 of the trigger are always zero.
0	R	Reserved for future use. Write as 0 to ensure future compatibility.

FIGURE 13

Count Register (WDOG_COUNT) – Read Only

Register : WDOG_COUNT Address : Address Base + 0x4C4 Access: Read

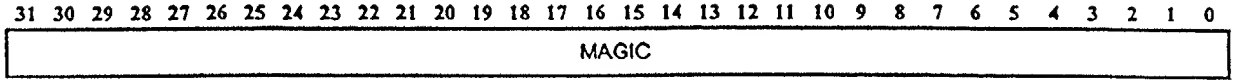


COUNT	R	Current value of watchdog count register.

FIGURE 14

Reload Register (WDOG_RELOAD) – Write Only

Register : WDOG_RELOAD Address : Address Base + 0x4C8 Access: Write



MAGIC	W	Magic value to reset watchdog.

FIGURE 15

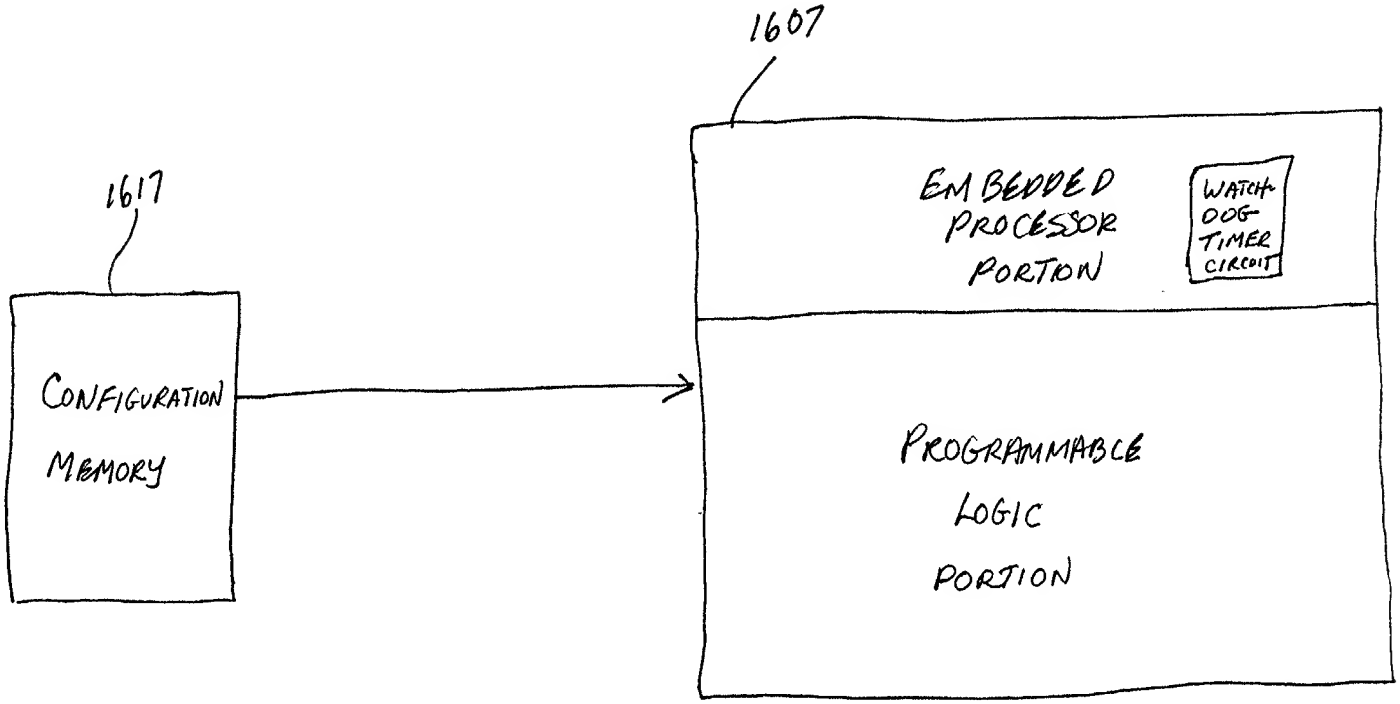

1607
1617
EMBEDDED PROCESSOR PORTION
WATCH-DOG TIMER CIRCUIT
CONFIGURATION MEMORY
PROGRAMMABLE LOGIC PORTION

FIGURE 16

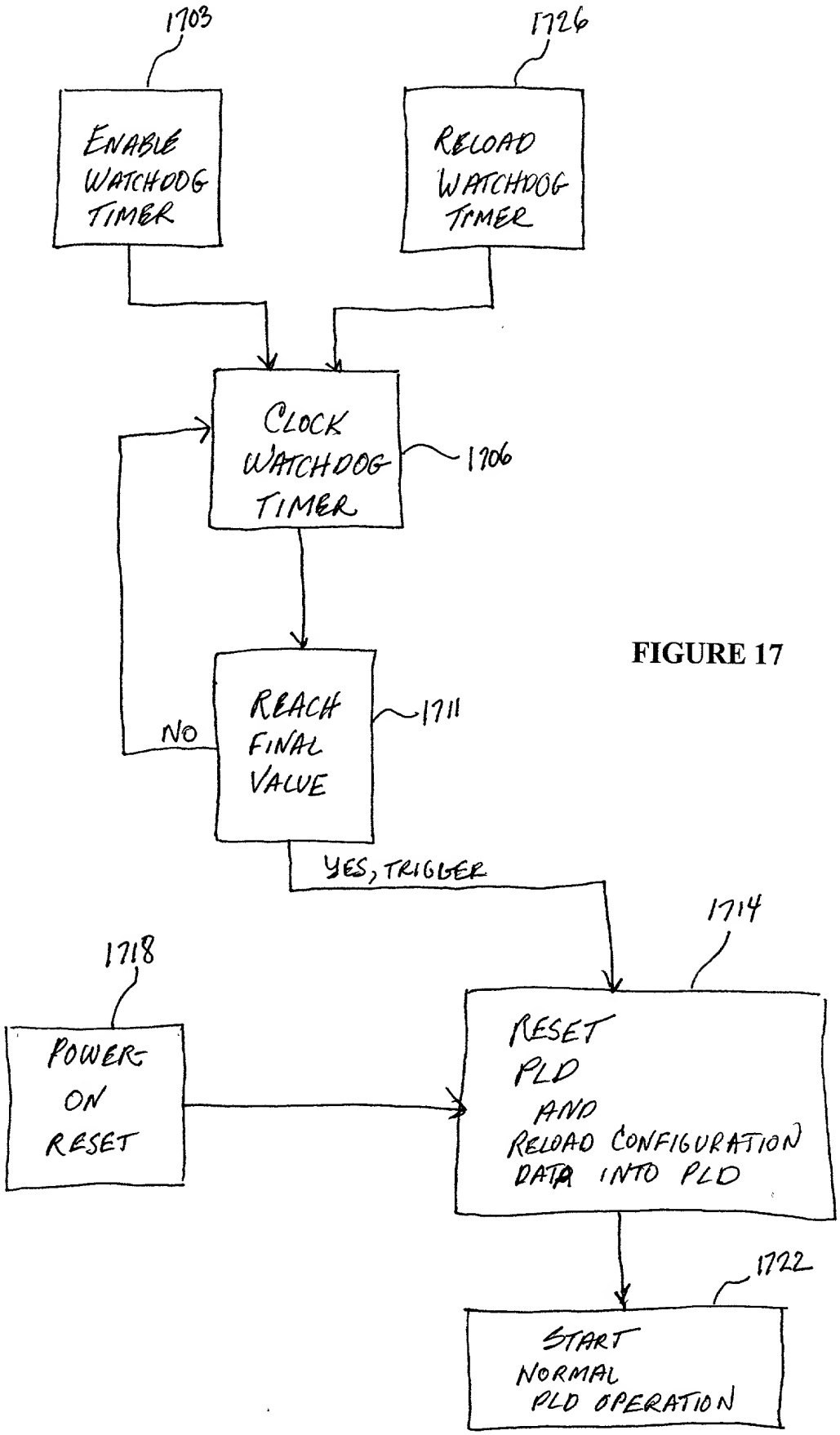

1703
ENABLE WATCHDOG TIMER
1726
RELOAD WATCHDOG TIMER
CLOCK WATCHDOG TIMER
1706
REACH FINAL VALUE
1711
NO
YES, TRIGGER
1714
1718
POWER-ON RESET
RESET PLD AND RELOAD CONFIGURATION DATA INTO PLD
1722
START NORMAL PLD OPERATION

FIGURE 17